INTEGRATED TECHNICAL EDUCATION CLUSTER
AT ALAMEERIA

J-601-1448
Electronic Principals

Lecture #3
BJT Transistors & DC Biasing

Instructor:
Dr. Ahmad El-Banna

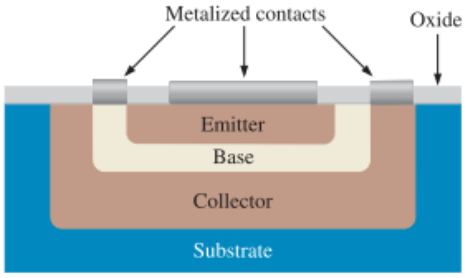
NOVEMBER 2014

Agenda

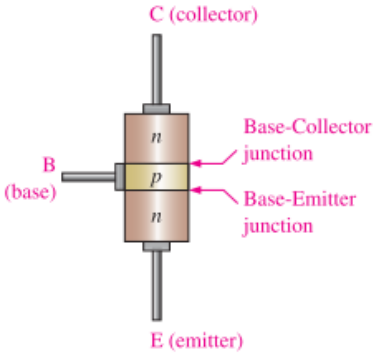
- Transistor Construction & Operation
- Transistor Configurations
- Transistor Testing & Terminal Identification
- Transistor DC Bias Configurations
- Design Operations
- Various BJT Circuits &Troubleshooting Techniques
- Practical Applications

Transistor Construction

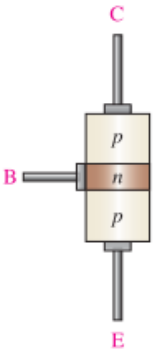
- Basic BJT Constructions



(a) Basic epitaxial planar structure

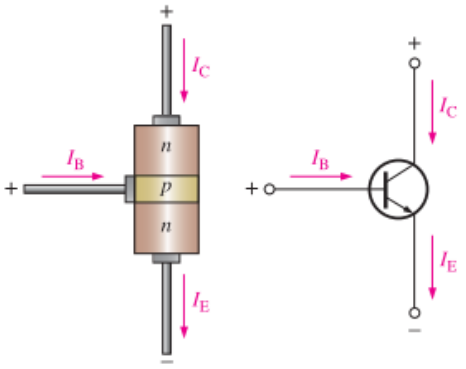


(b) *npn*

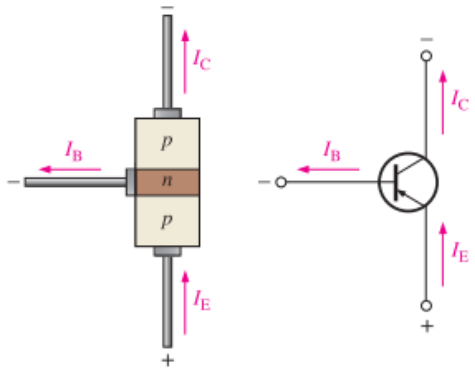


(c) *pnp*

- Basic BJT symbols and Currents



(a) *npn*

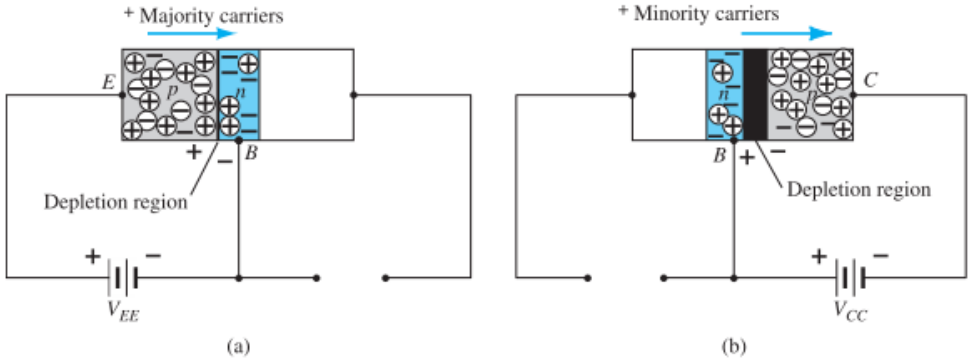


(b) *pnp*

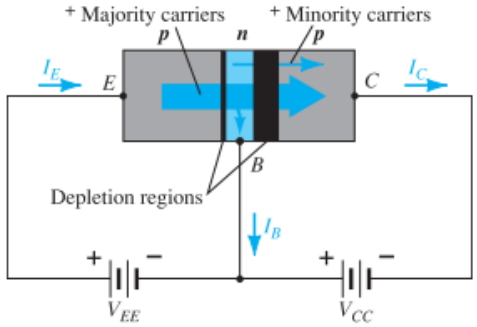
Transistor Operation

- Basic Operation using *pnp* transistor.

- Biasing a transistor:
  (a) forward-bias
  (b) reverse-bias.



- Majority and minority carrier flow of a *pnp* transistor.



$$I_E = I_C + I_B$$

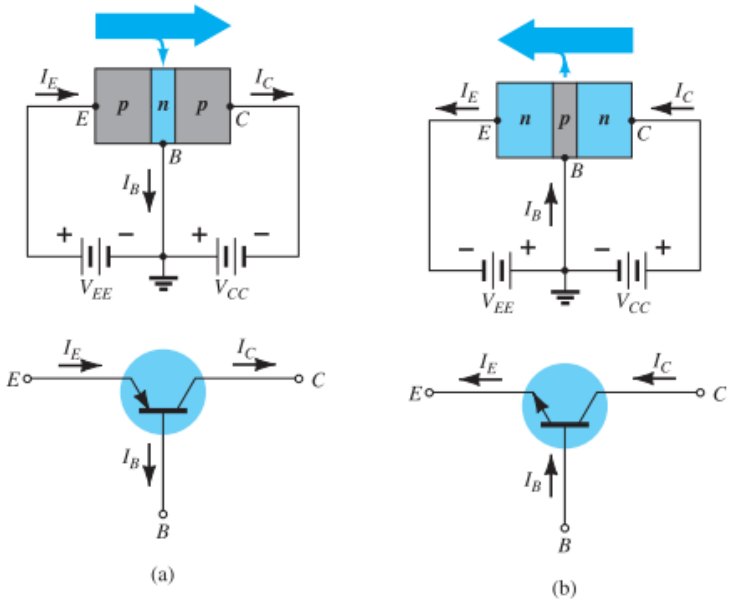
$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$

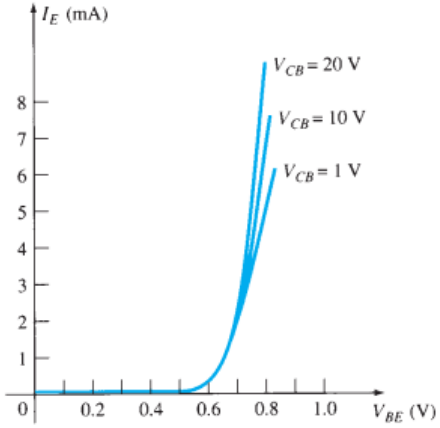
BJT CONFIGURATIONS

- Common Base
- Common Emitter
- Common Collector

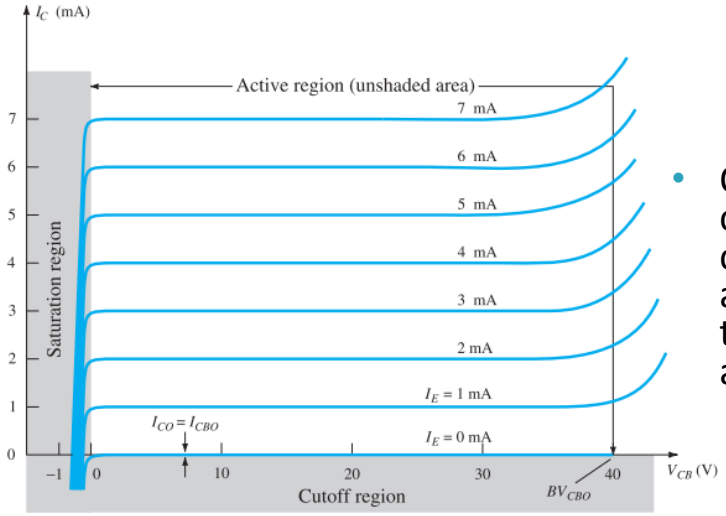
Configurations: Common Base

- Notation and symbols used with the common-base configuration: (a) pnp transistor; (b) npn transistor.





- Input or driving point characteristics for a common-base silicon transistor amplifier.



- Output or collector characteristics for a common-base transistor amplifier.

Configurations: Common Base..

- Formulas:

$$I_C \cong I_E$$

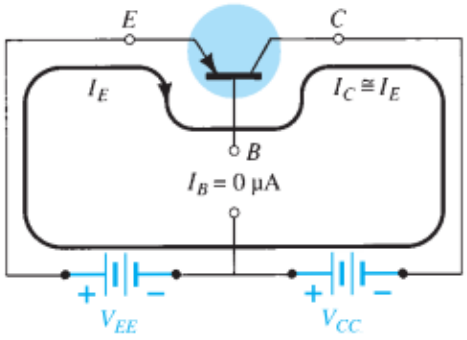
$$V_{BE} \cong 0.7\ \text{V}$$

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

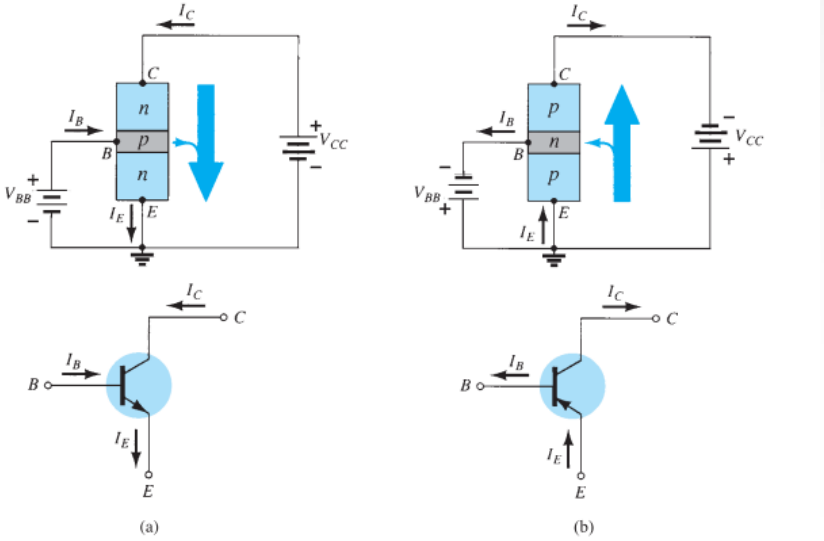
$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

- Biasing of a CB pnp tr. in the active region:

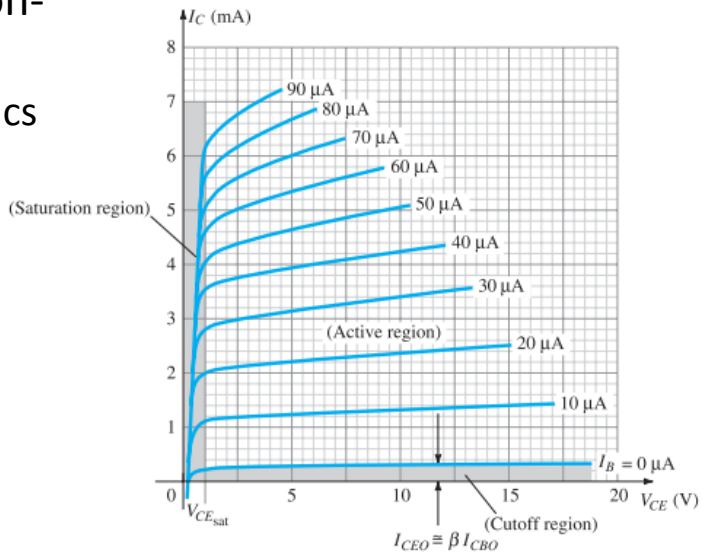


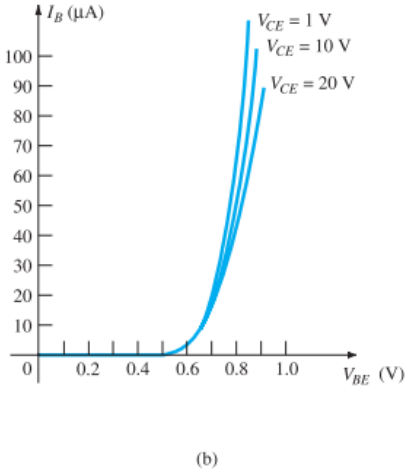
Configurations: Common Emitter

- Notation and symbols used with the common-emitter configuration:
  (a) pnp transistor
  (b) npn transistor.



- Characteristics of a silicon transistor in the common-emitter configuration:
  (a) collector characteristics
  (b) base characteristics.





Configurations: Common Emitter..

- Formulas:

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$I_{CEO} \cong \beta I_{CBO}$$

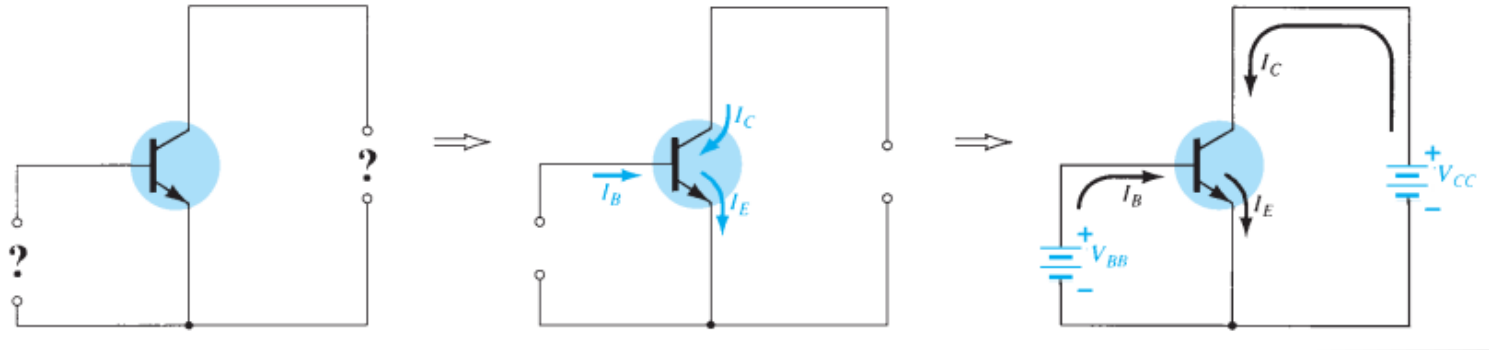
$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$I_C = \beta I_B$$

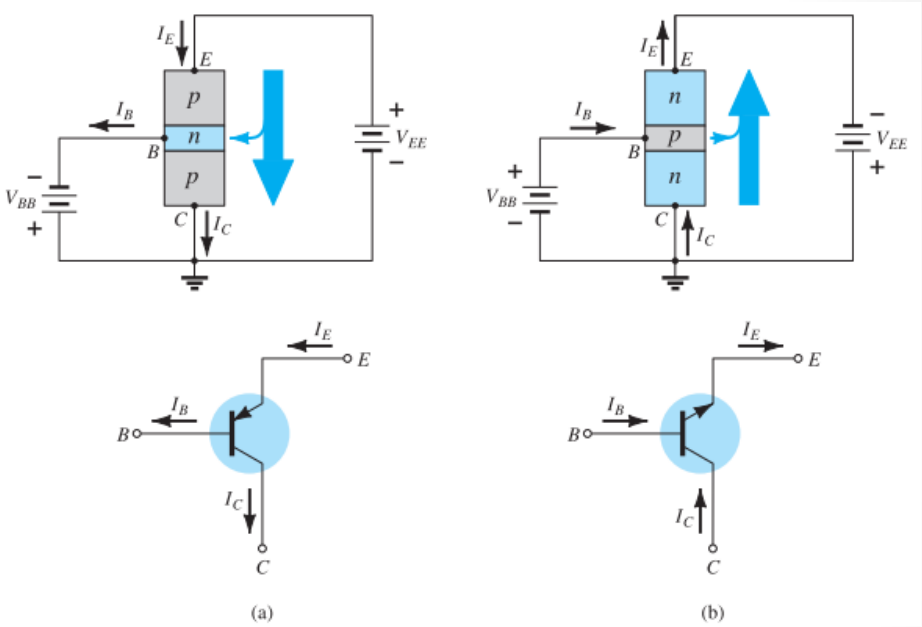
$$I_E = (\beta + 1) I_B$$

- Biasing of a CE npn tr. in the active region:

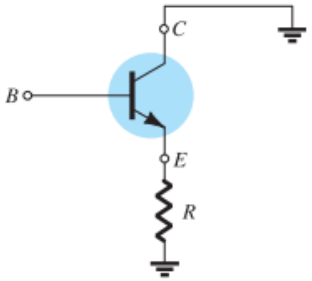


Configurations: Common Collector

- Notation and symbols used with the common-collector configuration: (a) pnp transistor; (b) npn transistor.



- Common-collector configuration used for impedance-matching purposes.



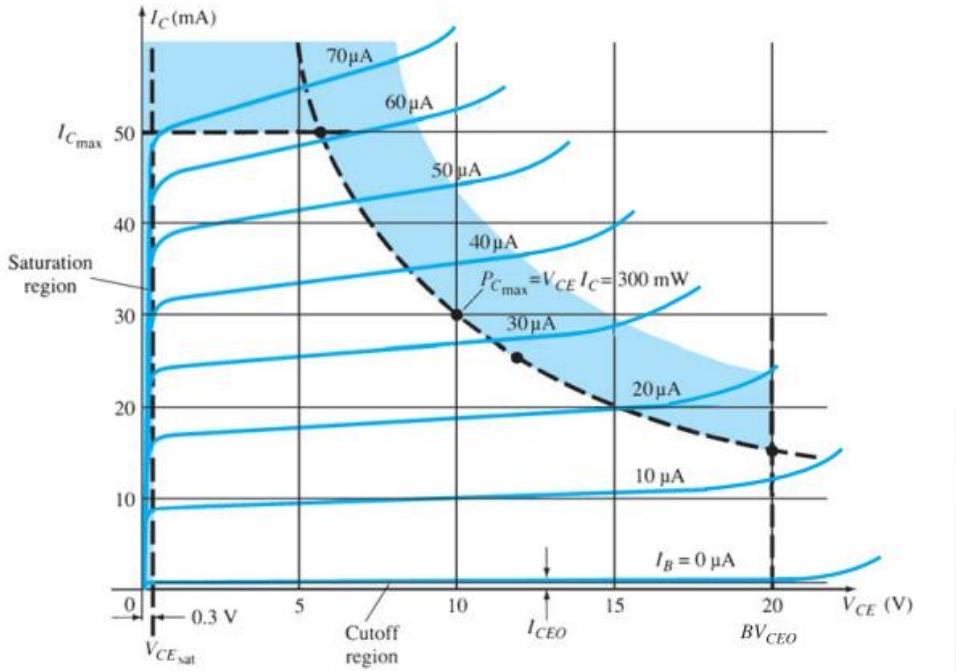
Configurations: Common Collector..

- Formulas:

$$P_{C_{max}} = V_{CE} I_C$$

$$I_{CEO} \leqq I_C \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq V_{CE} \leqq V_{CE_{max}}$$
$$V_{CE} I_C \leqq P_{C_{max}}$$

- Defining the linear (undistorted) region of operation for a transistor.



- Transistor Spec. Sheets
- Transistor Testing
- Transistor Casing and terminals identification
- Transistor Development

PRACTICAL VIEW

Transistor Specification Sheets

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

FAIRCHILD
SEMICONDUCTOR ™

2N4123

TO-92

General Purpose Transistor NPN Silicon

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

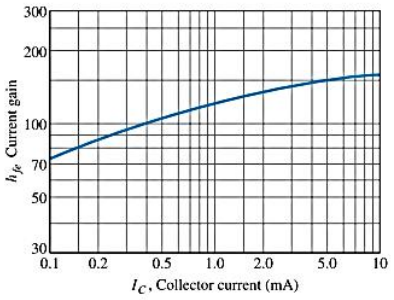
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0$ mAdc, $I_E = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10$ µAdc, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ µAdc, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current ($V_{BE} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 2.0$ mAdc, $V_{CE} = 1.0$ Vdc) ($I_C = 50$ mAdc, $V_{CE} = 1.0$ Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{BE(sat)}$	–	0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, f = 100 MHz)	f_T	250		MHz
Output Capacitance ($V_{CB} = 5.0$ Vdc, $I_E = 0$, f = 100 MHz)	C_{obo}	–	4.0	pF
Input Capacitance ($V_{BE} = 0.5$ Vdc, $I_C = 0$, f = 100 kHz)	C_{ibo}	–	8.0	pF
Collector-Base Capacitance ($I_E = 0$, $V_{CB} = 5.0$ V, f = 100 kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, f = 1.0 kHz)	h_{fe}	50	200	–
Current Gain – High Frequency ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, f = 100 MHz) ($I_C = 2.0$ mAdc, $V_{CE} = 10$ V, f = 1.0 kHz)	h_{fe}	2.5 50	– 200	–
Noise Figure ($I_C = 100$ µAdc, $V_{CE} = 5.0$ Vdc, $R_S = 1.0$ k ohm, f = 1.0 kHz)	NF	–	6.0	dB

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%

Transistor Specification Sheets..

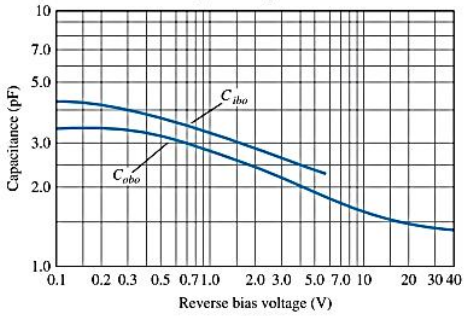
h PARAMETERS
V_{CE} = 10 V, f = 1 kHz, T_A = 25°C

Figure 1 – Current Gain



(b)

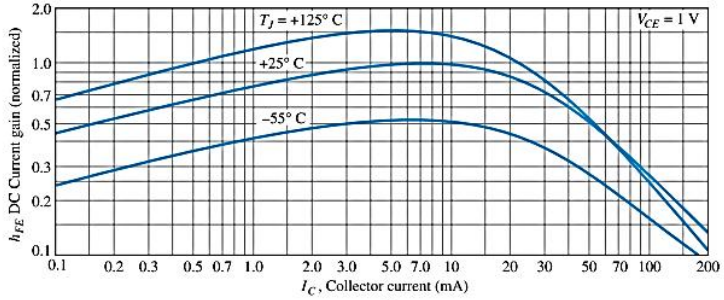
Figure 3 – Capacitance



(d)

STATIC CHARACTERISTICS

Figure 2 – DC Current Gain



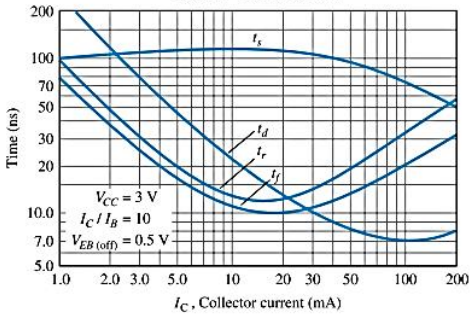
(c)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

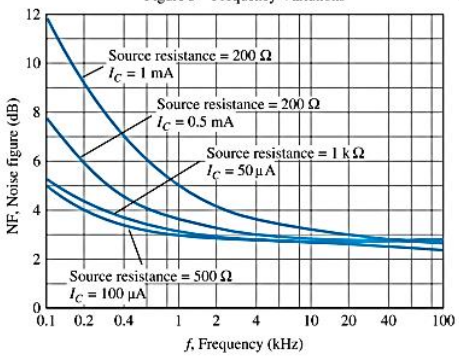
(V_{CE} = 5 Vdc, T_A = 25°C)
Bandwidth = 1.0 Hz

Figure 4 – Switching Times



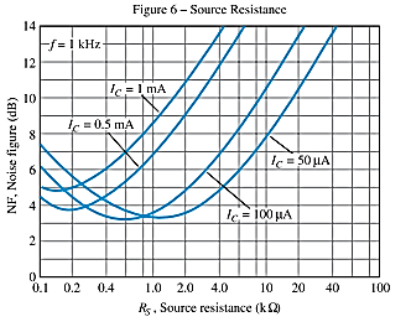
(e)

Figure 5 – Frequency Variations



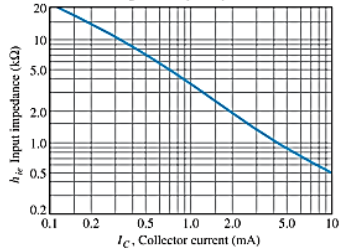
(f)

Figure 6 – Source Resistance



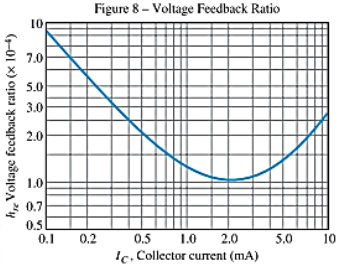
(g)

Figure 7 – Input Impedance



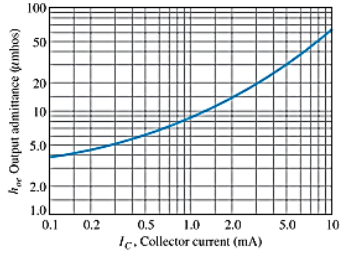
(h)

Figure 8 – Voltage Feedback Ratio



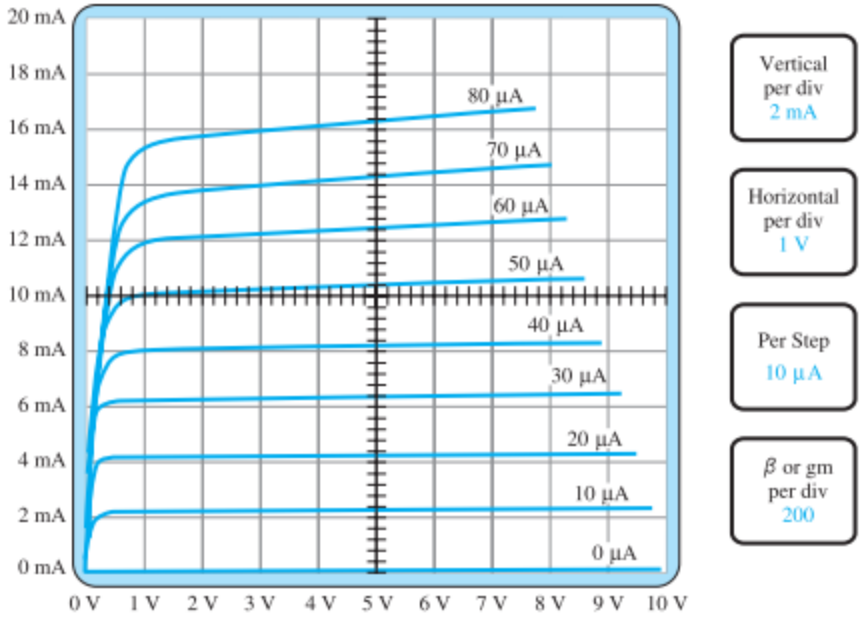
(i)

Figure 9 – Output Admittance

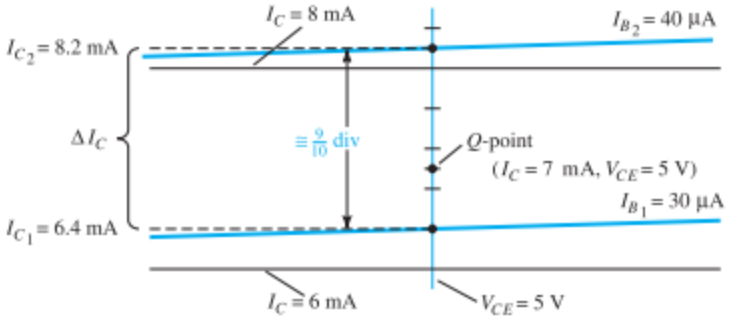


(j)

Transistor Testing using Curve Tracer



Curve tracer response to 2N3904 npn transistor.



Determining β_{ac} for the transistor characteristics of 2N3904 npn transistor at $I_C = 7$ mA and $V_{CE} = 5$ V.

$$\beta_{ac} = \frac{9}{10}\,\cancel{\text{div}}\left(\frac{200}{\cancel{\text{div}}}\right) = \mathbf{180}$$

- Check the beta value:

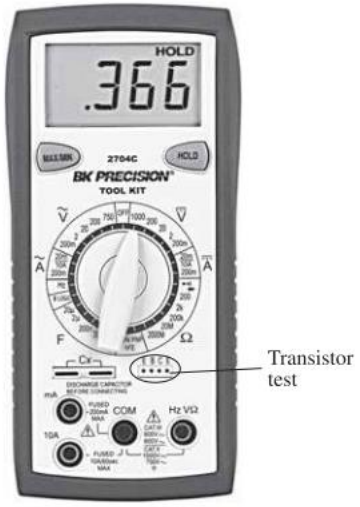
$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$$

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_1} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{8.2\text{ mA} - 6.4\text{ mA}}{40\,\mu\text{A} - 30\,\mu\text{A}}$$

$$= \frac{1.8\text{ mA}}{10\,\mu\text{A}} = \mathbf{180}$$

Transistor Testing using Transistor Tester

- Transistor testers:
  (a) digital meter
  (b) dedicated testers.

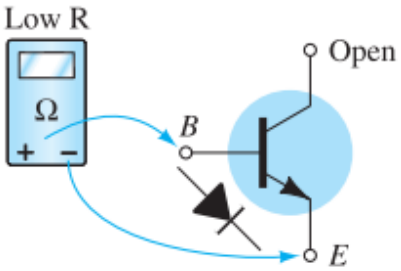


(a)

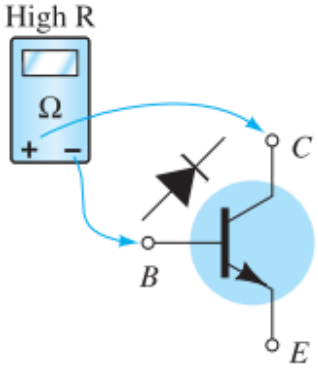
(b)

Transistor Testing using Ohmmeter

- Checking the forward-biased base-to-emitter junction of an *npn* transistor.



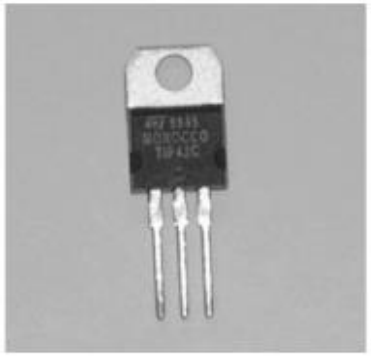
- Checking the reverse-biased base-to-collector junction of an *npn* transistor.



Transistor Casing

- Various types of general-purpose or switching transistors:
  (a) low power
  (b) medium power
  (c) medium to high power.

(a)

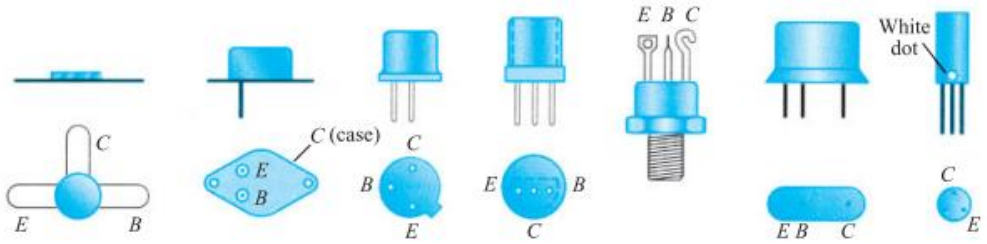


(b)

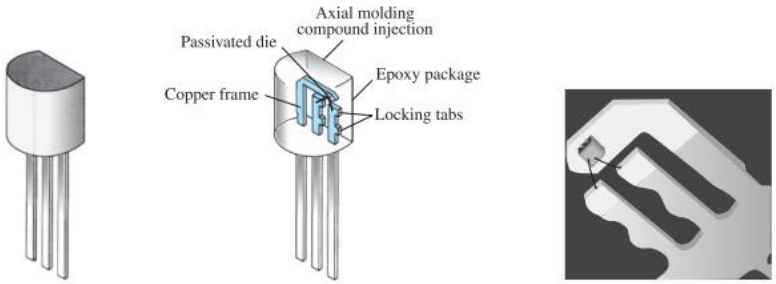
(c)

Terminal Identification

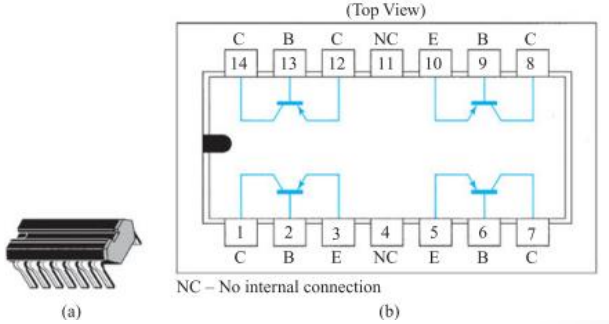
- Transistor terminal identification.



- Internal construction of a Fairchild transistor in a TO-92 package.



- Type Q2T2905 Texas Instruments quad pnp silicon transistor:
  (a) Appearance
  (b) pin connections.



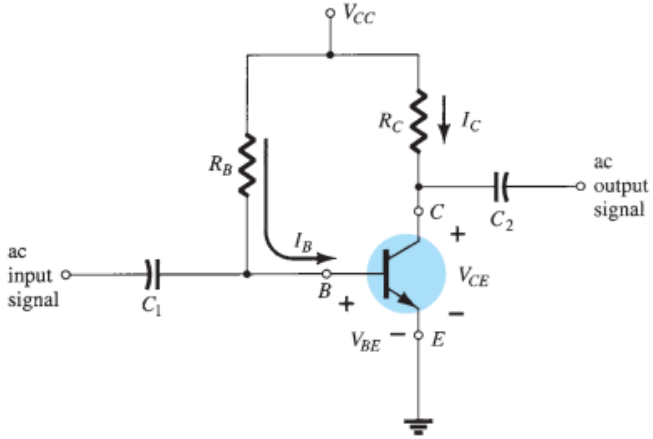
- Fixed-Bias Configuration
- Voltage-Divider Bias Configuration
- Emitter-Follower Configuration

TRANSISTOR DC BIAS CONFIGURATIONS

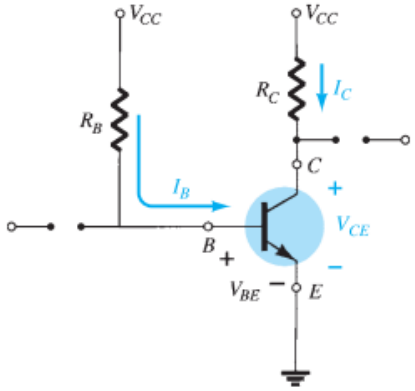
- ***Biasing*** means applying of dc voltages to establish a fixed level of current and voltage. >>> Q-Point

Fixed-Bias Configuration

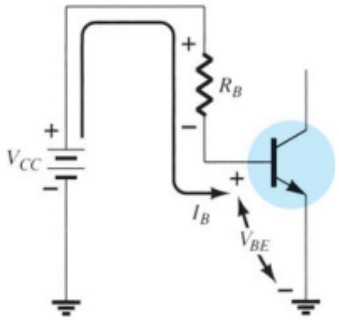
- Fixed-bias circuit.



- DC equivalent ct.



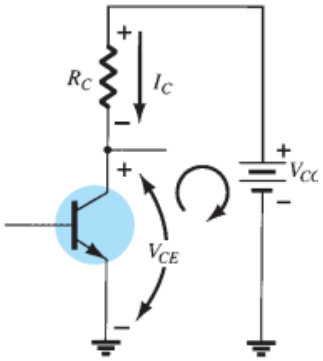
- Base–emitter loop.



$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

- Collector–emitter loop.



$$I_C = \beta I_B$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_C$$

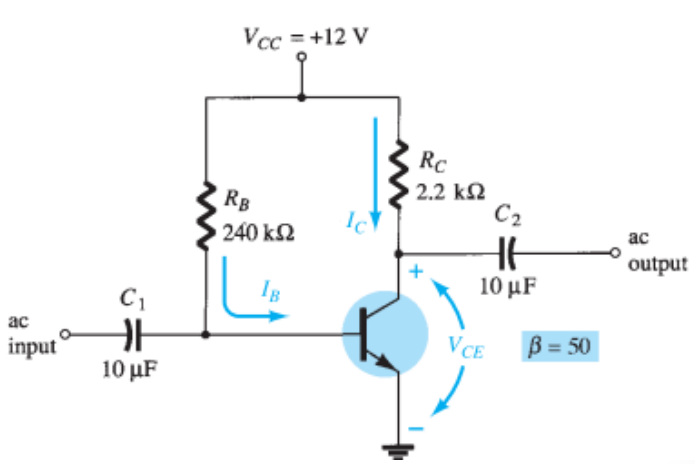
$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

Fixed-Bias Configuration Example

EXAMPLE 4.1 Determine the following for the fixed-bias configuration

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.



Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

b. Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

c. $V_B = V_{BE} = \mathbf{0.7\ V}$
$V_C = V_{CE} = \mathbf{6.83\ V}$

d. Using double-subscript notation yields
$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Fixed-Bias Configuration …

- **Load Line Analysis**

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - (0)R_C$$

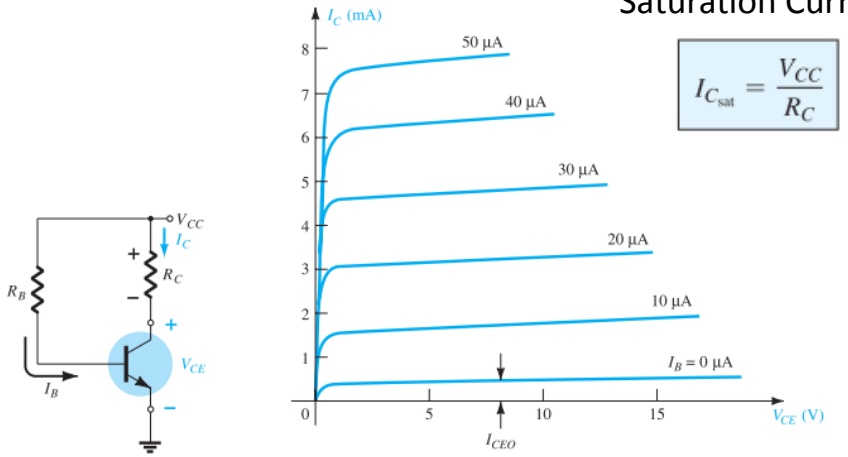
$$V_{CE} = V_{CC}|_{I_C=0\,\text{mA}}$$

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0\,\text{V}}$$

Saturation Current

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$



Load-line analysis: (a) the network; (b) the device characteristics.

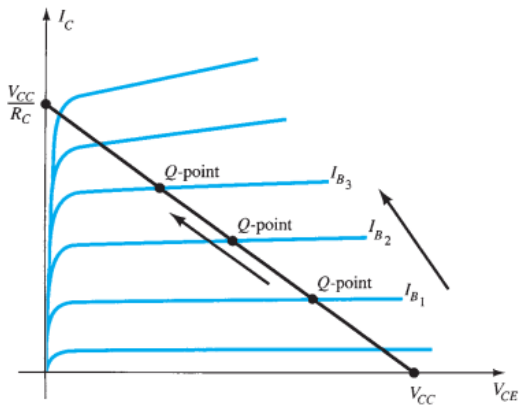


FIG. 4.13
Movement of the Q-point with increasing level of I_B.

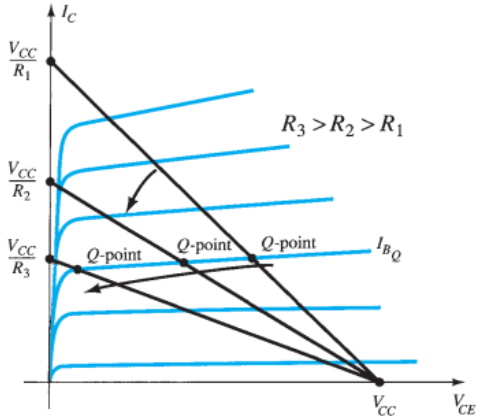


FIG. 4.14
Effect of an increasing level of R_C on the load line and the Q-point.

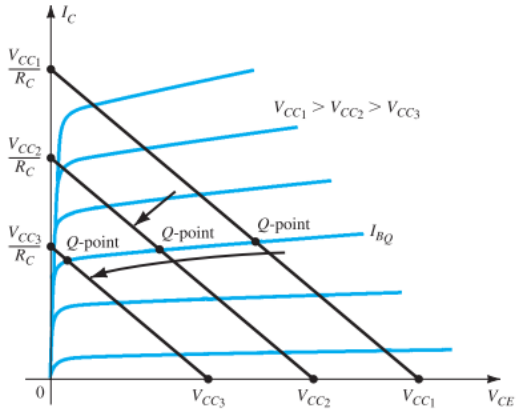
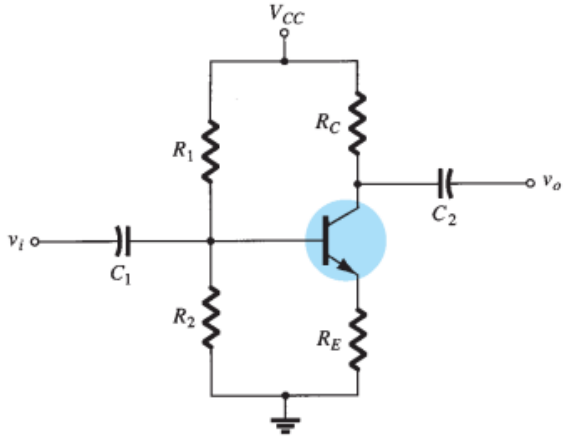


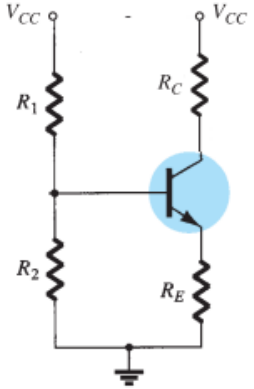
FIG. 4.15
Effect of lower values of V_{CC} on the load line and the Q-point.

Voltage-Divider Configuration

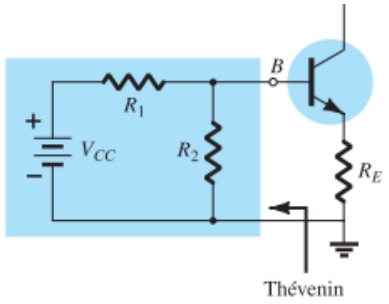
- Voltage-divider bias configuration.

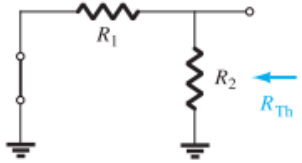


- DC components of the voltage-divider configuration.

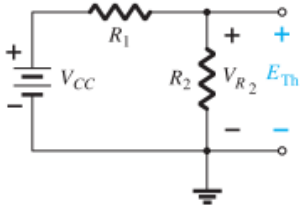


- Exact Analysis

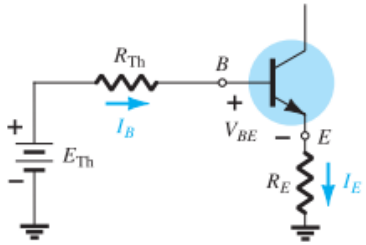




$$R_{Th} = R_1 \| R_2$$



$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

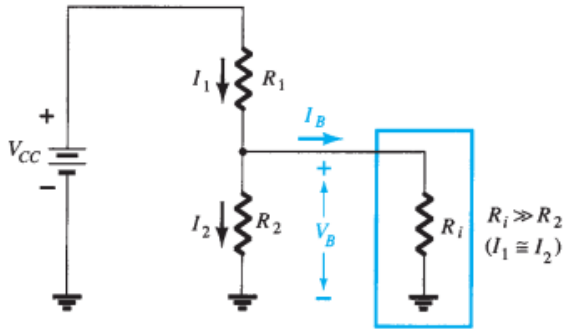


$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Voltage-Divider Configuration

- Approximate Analysis



$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_i = (\beta + 1)R_E \cong \beta R_E$$

$$\beta R_E \geq 10R_2$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

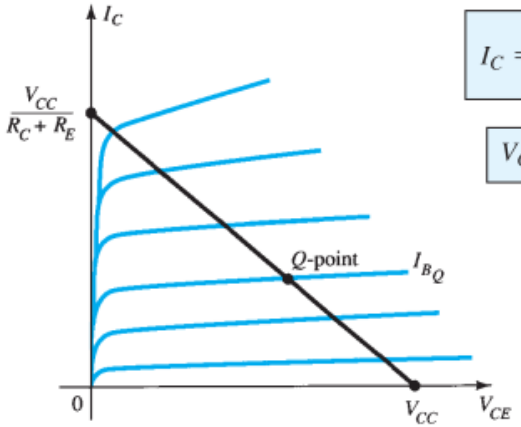
$$I_{C_Q} \cong I_E$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

- Transistor Saturation

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

- Load-Line Analysis



$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\,V}$$

$$V_{CE} = V_{CC}|_{I_C=0\,mA}$$

Voltage-Divider Configuration Example

EXAMPLE 4.11 Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) *will not be satisfied* and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

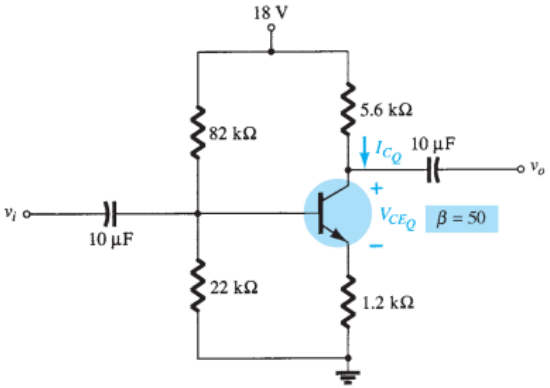


FIG. 4.37
Voltage-divider configuration for Example 4.11.

Solution: Exact analysis:

Eq. (4.33):

$$\beta R_E \geq 10R_2$$
$$(50)(1.2\,\text{k}\Omega) \geq 10(22\,\text{k}\Omega)$$
$$60\,\text{k}\Omega \not\geq 220\,\text{k}\Omega \text{ (not satisfied)}$$

$$R_{\text{Th}} = R_1 \| R_2 = 82\,\text{k}\Omega \| 22\,\text{k}\Omega = 17.35\,\text{k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\,\text{k}\Omega(18\,\text{V})}{82\,\text{k}\Omega + 22\,\text{k}\Omega} = 3.81\,\text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81\,\text{V} - 0.7\,\text{V}}{17.35\,\text{k}\Omega + (51)(1.2\,\text{k}\Omega)} = \frac{3.11\,\text{V}}{78.55\,\text{k}\Omega} = 39.6\,\mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(39.6\,\mu\text{A}) = \mathbf{1.98\,mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 18\,\text{V} - (1.98\,\text{mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$
$$= \mathbf{4.54\,V}$$

Approximate analysis:

$$V_B = E_{\text{Th}} = 3.81\,\text{V}$$
$$V_E = V_B - V_{BE} = 3.81\,\text{V} - 0.7\,\text{V} = 3.11\,\text{V}$$
$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11\,\text{V}}{1.2\,\text{k}\Omega} = \mathbf{2.59\,mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 18\,\text{V} - (2.59\,\text{mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$
$$= \mathbf{3.88\,V}$$

Comparing the exact and approximate approaches.

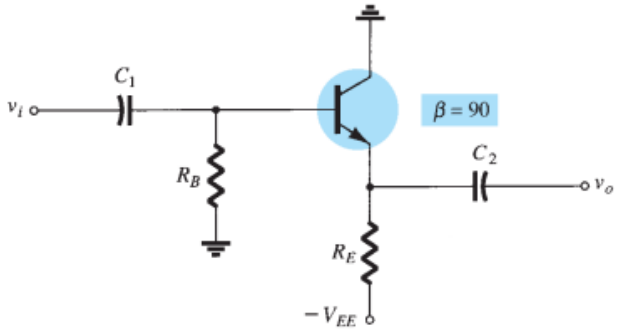
	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, whereas V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

$$\beta R_E \geq 10R_2 \qquad \textbf{(4.33)}$$

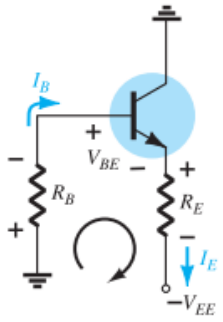
Emitter-Follower Configuration

- Common-collecter (emitter-follower) configuration.



- dc equivalent ct

i/p ct



$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$I_B R_B + (\beta + 1) I_B R_E = V_{EE} - V_{BE}$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

o/p ct

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

EXAMPLE 4.16 Determine V_{CE_Q} and I_{E_Q} for the network of Fig. 4.48.

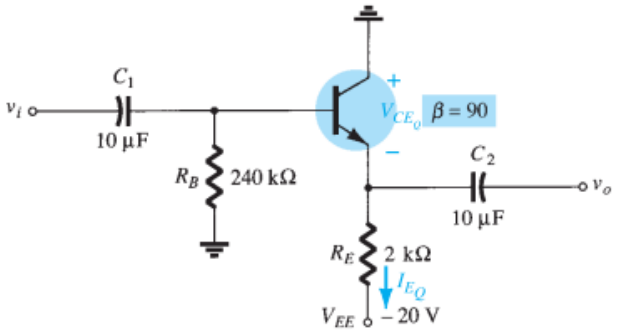


FIG. 4.48
Example 4.16.

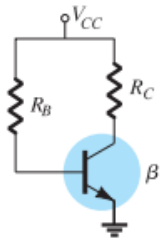
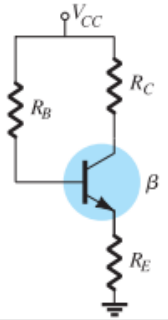
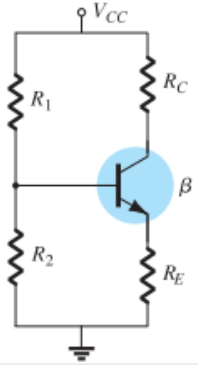
Solution:

Eq. 4.44:
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega + (90 + 1)2\text{ k}\Omega} = \frac{19.3\text{ V}}{240\text{ k}\Omega + 182\text{ k}\Omega}$$
$$= \frac{19.3\text{ V}}{422\text{ k}\Omega} = 45.73\ \mu\text{A}$$

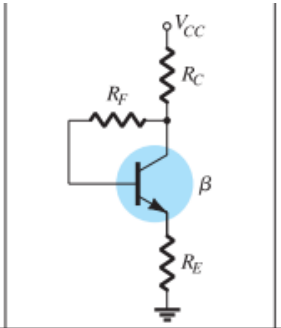
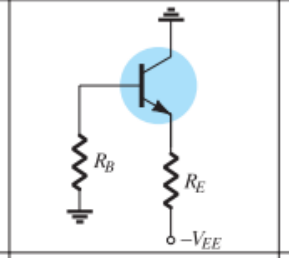
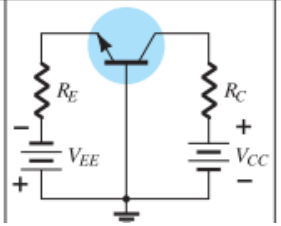
and Eq. 4.45:
$$V_{CE_Q} = V_{EE} - I_E R_E$$
$$= V_{EE} - (\beta + 1) I_B R_E$$
$$= 20\text{ V} - (90 + 1)(45.73\ \mu\text{A})(2\text{ k}\Omega)$$
$$= 20\text{ V} - 8.32\text{ V}$$
$$= \mathbf{11.68\text{ V}}$$
$$I_{E_Q} = (\beta + 1) I_B = (91)(45.73\ \mu\text{A})$$
$$= 4.16\text{ mA}$$

Summary Table

BJT Bias Configurations

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Voltage-divider bias		EXACT: $R_{Th} = R_1 \| R_2, E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$ $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$ APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$

Summary Table..

Collector-feedback		$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Emitter-follower		$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
Common-base		$I_E = \frac{V_{EE} - V_{BE}}{R_E}$ $I_B = \frac{I_E}{\beta + 1}, I_C = \beta I_B$ $V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$ $V_{CB} = V_{CC} - I_C R_C$

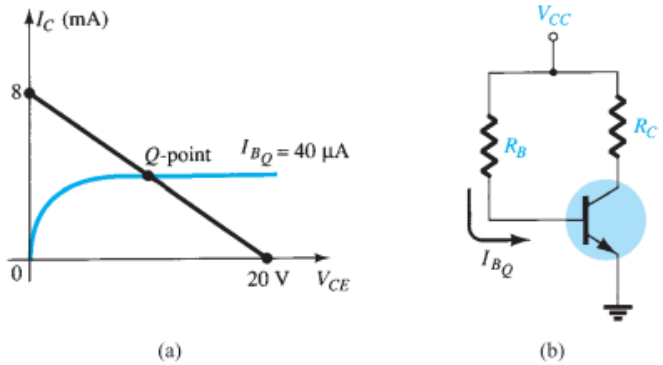
DESIGN OPERATION

Design Operations

- The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.
- The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.
- Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design.

Design Operations Example

EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b.



Solution: From the load line

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ V}{8\ mA} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ V - 0.7\ V}{40\ \mu A} = \frac{19.3\ V}{40\ \mu A} = \mathbf{482.5\ k\Omega}$$

Standard resistor values are

$$R_C = 2.4\ k\Omega$$

$$R_B = 470\ k\Omega$$

Using standard resistor values gives

$$I_B = 41.1\ \mu A$$

which is well within 5% of the value specified.

VARIOUS BJT CIRCUITS

- MULTIPLE BJT NETWORKS
- CURRENT MIRRORS
- CURRENT SOURCE CIRCUITS
  - Bipolar Transistor Constant-Current Source
  - Transistor/Zener Constant-Current Source
- PNP TRANSISTORS
- TRANSISTOR SWITCHING NETWORKS

MULTIPLE BJT NETWORKS

- **R–C coupling**

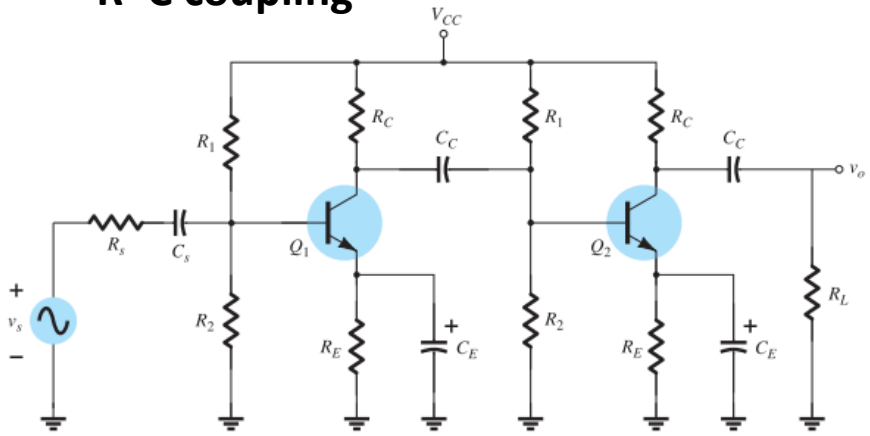
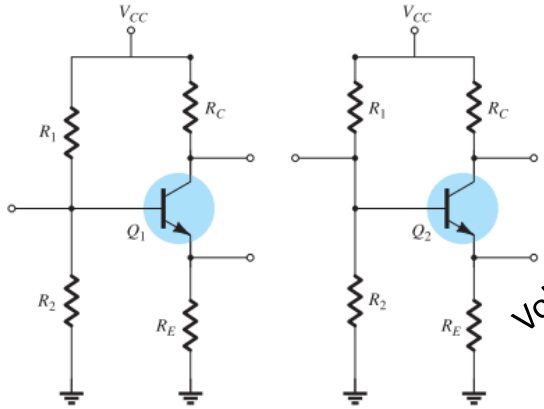


FIG. 4.64
R–C coupled BJT amplifiers.



Voltage divider ;)

FIG. 4.65
DC equivalent of Fig. 4.64.

- **Darlington configuration**

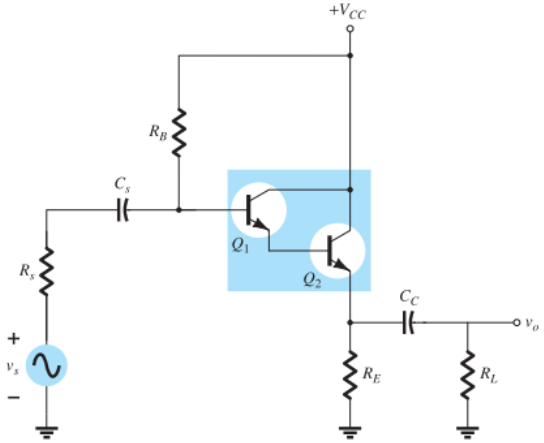


FIG. 4.66
Darlington amplifier.

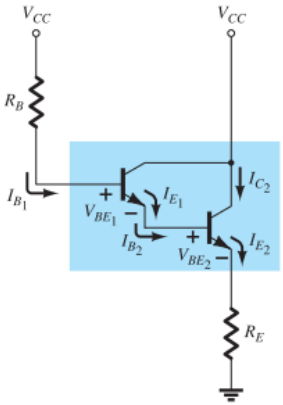


FIG. 4.67
DC equivalent of Fig. 4.66.

$$\beta_D = \beta_1\beta_2$$

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + (\beta_D + 1)R_E}$$

$$V_{BE_D} = V_{BE_1} + V_{BE_2}$$

$$I_{B_1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E}$$

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1}$$

$$V_{E_2} = I_{E_2}R_E$$

$$V_{C_2} = V_{CC}$$

$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$V_{CE_2} = V_{CC} - V_{E_2}$$

CURRENT MIRRORS

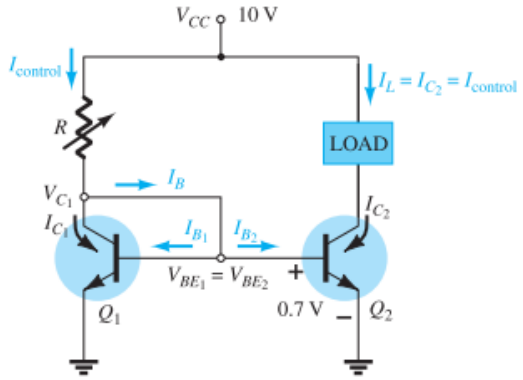


FIG. 4.74
Current mirror using back-to-back BJTs.

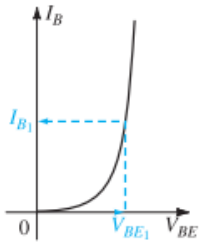


FIG. 4.75
Base characteristics for transistor Q_1 (and Q_2).

$$I_{control} = I_{C_1} + I_B = I_{C_1} + 2I_{B_1}$$
$$I_{C_1} = \beta_1 I_{B_1}$$
$$I_{control} = \beta_1 I_{B_1} + 2I_{B_1} = (\beta_1 + 2)I_{B_1}$$

β_1 is typically $\gg 2$, $I_{control} \cong \beta_1 I_{B_1}$

$$\boxed{I_{B_1} = \frac{I_{control}}{\beta_1}}$$

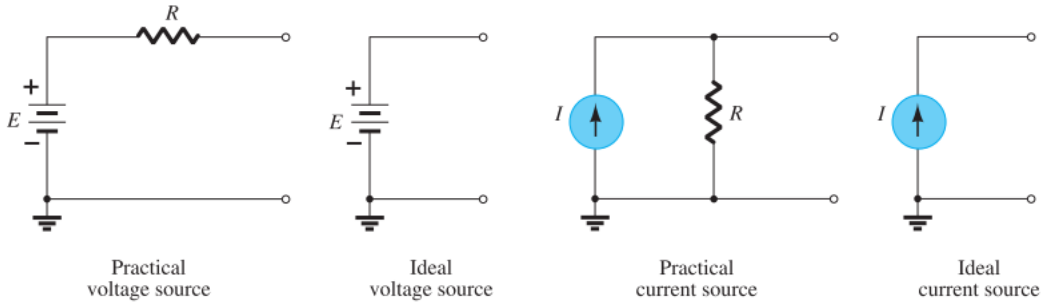
$$I_L = I_{C_2} = \beta I_{B_2}$$

$$\boxed{I_{control} = \frac{V_{CC} - V_{BE}}{R}}$$

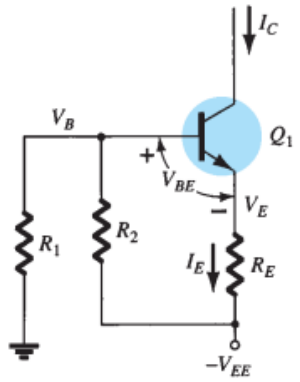
$I_L \uparrow I_{C_2} \uparrow I_{B_2} \uparrow V_{BE_2} \uparrow V_{CE_1} \updownarrow, I_R \downarrow, I_B \downarrow, I_{B_2} \downarrow I_{C_2} \downarrow I_L \downarrow$

Note

CURRENT SOURCE CIRCUITS



- **Bipolar Transistor Constant-Current Source**



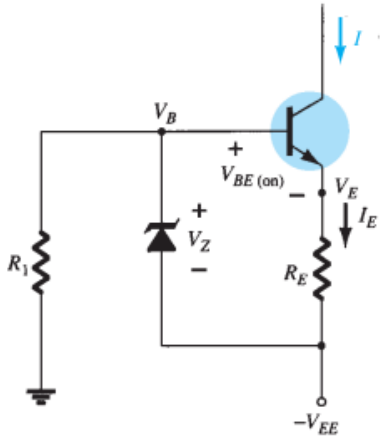
$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE})$$

$$V_E = V_B - 0.7\ \text{V}$$

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C$$

FIG. 4.81
Discrete constant-current source.

- **Transistor/Zener Constant-Current Source**



$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E}$$

FIG. 4.83
Constant-current circuit using Zener diode.

pnp TRANSISTORS

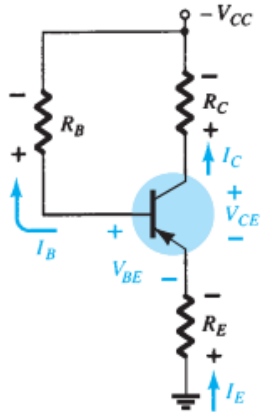


FIG. 4.85
pnp transistor in an emitter-stabilized configuration.

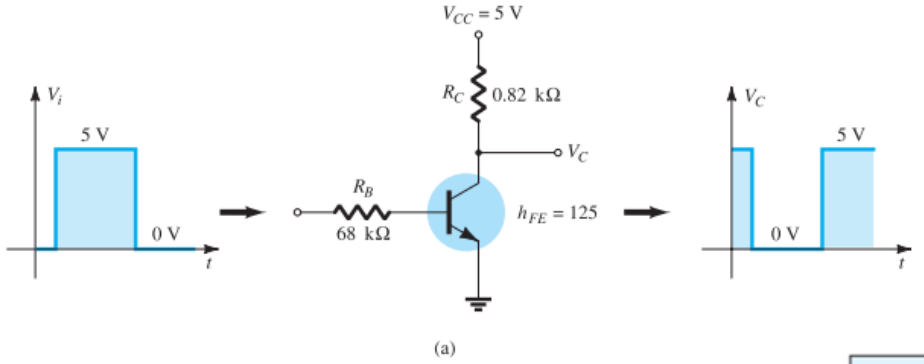
$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E}$$

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

TRANSISTOR SWITCHING NETWORKS

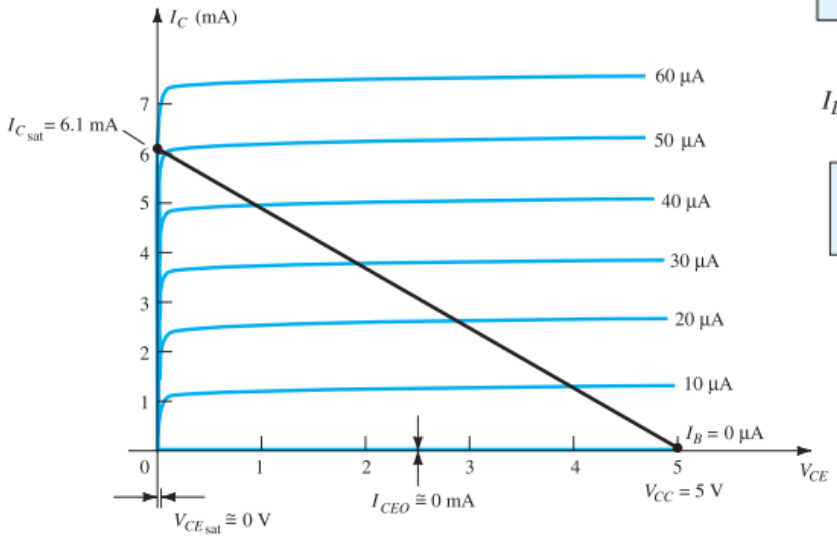


(a)

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

$$I_B > \frac{I_{C_{sat}}}{\beta_{dc}}$$



(b)

FIG. 4.87
Transistor inverter.

TRANSISTOR SWITCHING NETWORKS..

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}$$

and is depicted in Fig. 4.88.

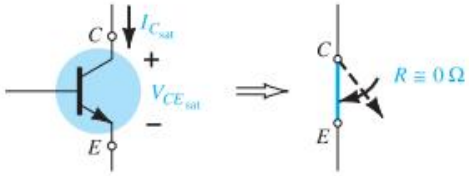


FIG. 4.88
Saturation conditions and the resulting terminal resistance.

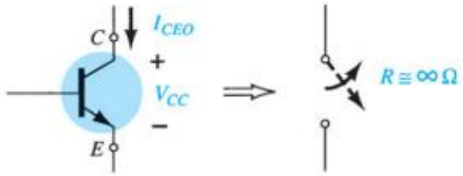


FIG. 4.89
Cutoff conditions and the resulting terminal resistance.

Using a typical average value of $V_{CE_{sat}}$ such as 0.15 V gives

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}} = \frac{0.15\text{ V}}{6.1\text{ mA}} = 24.6\,\Omega$$

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{0\text{ mA}} = \infty\,\Omega$$

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{10\,\mu\text{A}} = 500\text{ k}\Omega$$

$$t_{on} = t_r + t_d$$

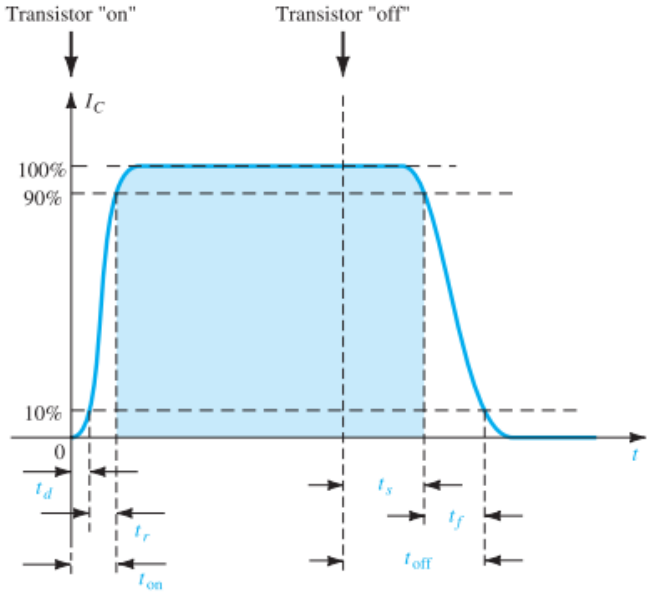


FIG. 4.91
Defining the time intervals of a pulse waveform.

$$t_{off} = t_s + t_f$$

TROUBLESHOOTING TECHNIQUES

TROUBLESHOOTING TECHNIQUES

- For an “on” transistor, the voltage V_{BE} should be in the neighborhood of 0.7 V.
- For the typical transistor amplifier in the active region, V_{CE} is usually about 25% to 75% of V_{CC}.

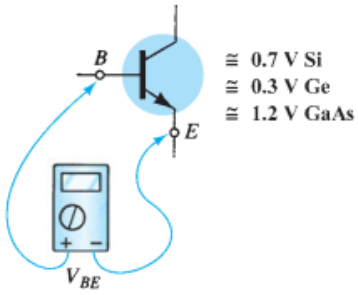


FIG. 4.92
Checking the dc level of V_{BE}.

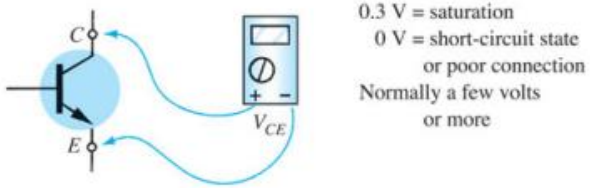


FIG. 4.93
Checking the dc level of V_{CE}.

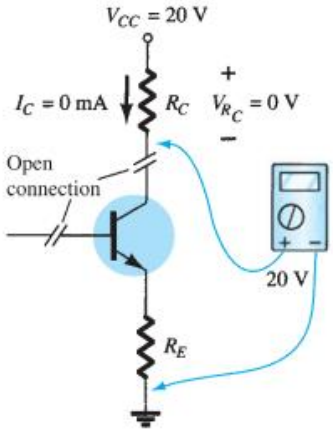


FIG. 4.94
Effect of a poor connection or damaged device.

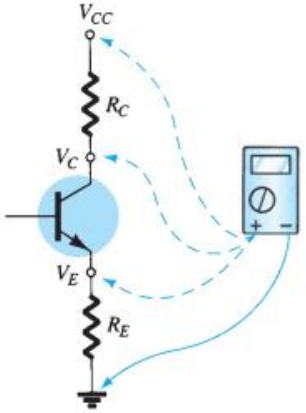


FIG. 4.95
Checking voltage levels with respect to ground.

PRACTICAL APPLICATION

- BJT Diode Usage and Protective Capabilities
- Relay Driver
- Alarm System with a CCS
- Voltage Level Indicator
- Logic Gates

Practical Application

- BJT Diode Usage and Protective Capabilities

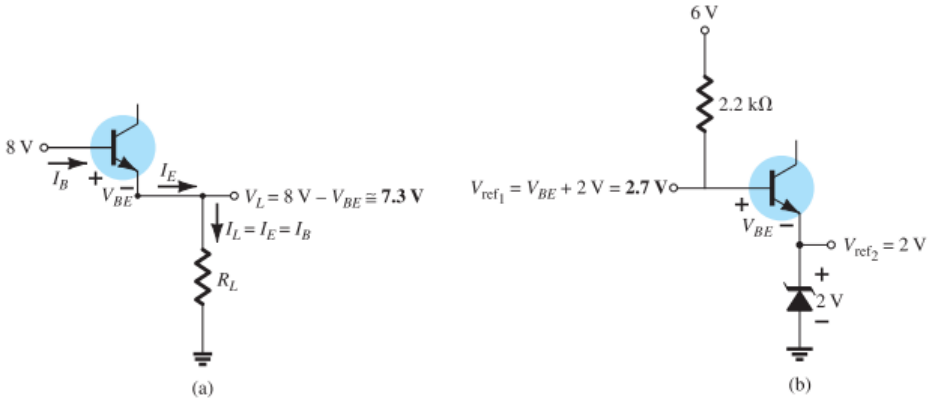


FIG. 4.102

BJT applications as a diode: (a) simple series diode circuit; (b) setting a reference level.

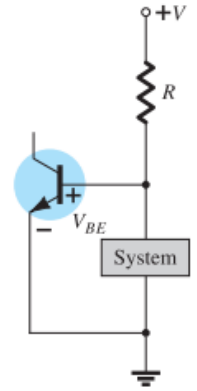


FIG. 4.103

Acting as a protective device.

- Relay Driver

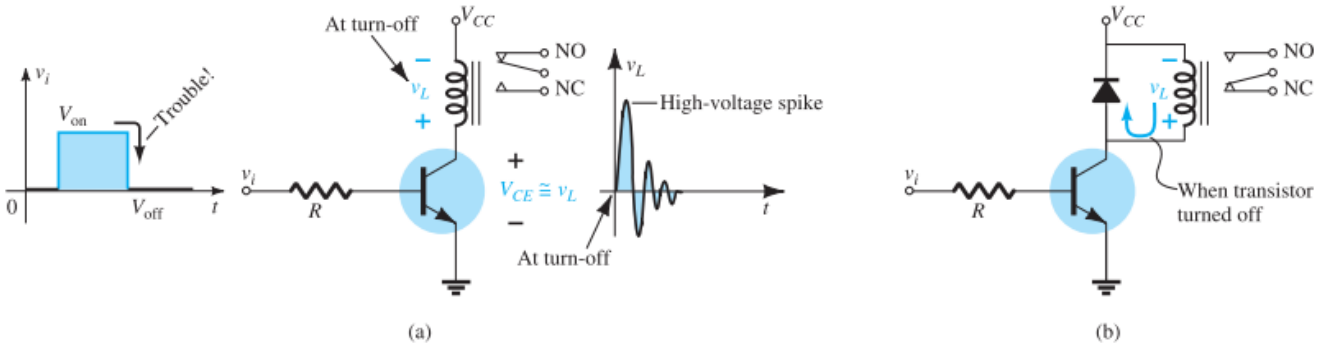


FIG. 4.104

Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.

Practical Application…

- Alarm System with a CCS

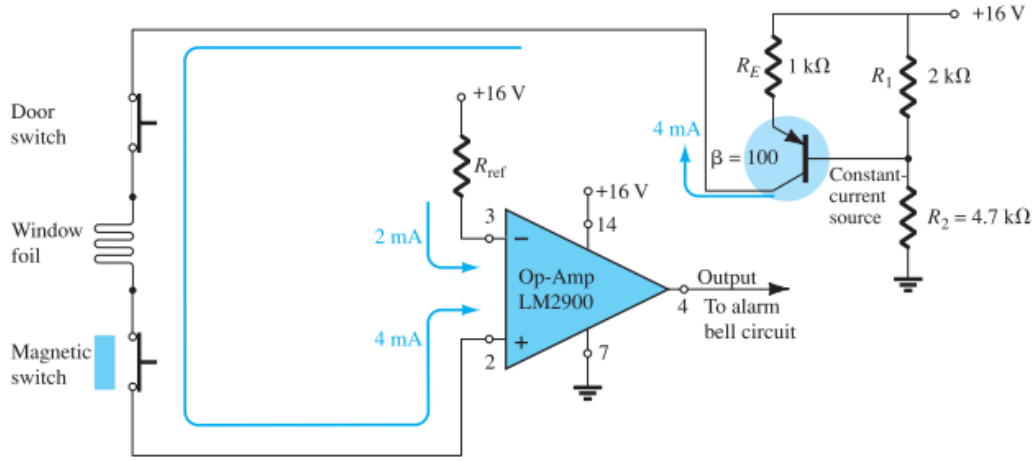


FIG. 4.108

An alarm system with a constant-current source and an op-amp comparator.

- Voltage Level Indicator

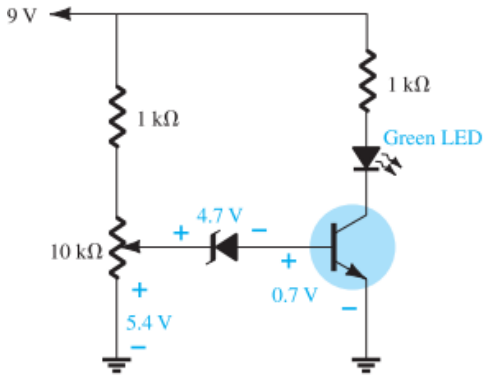


FIG. 4.112

Voltage level indicator.

Practical Application….

- Logic Gates

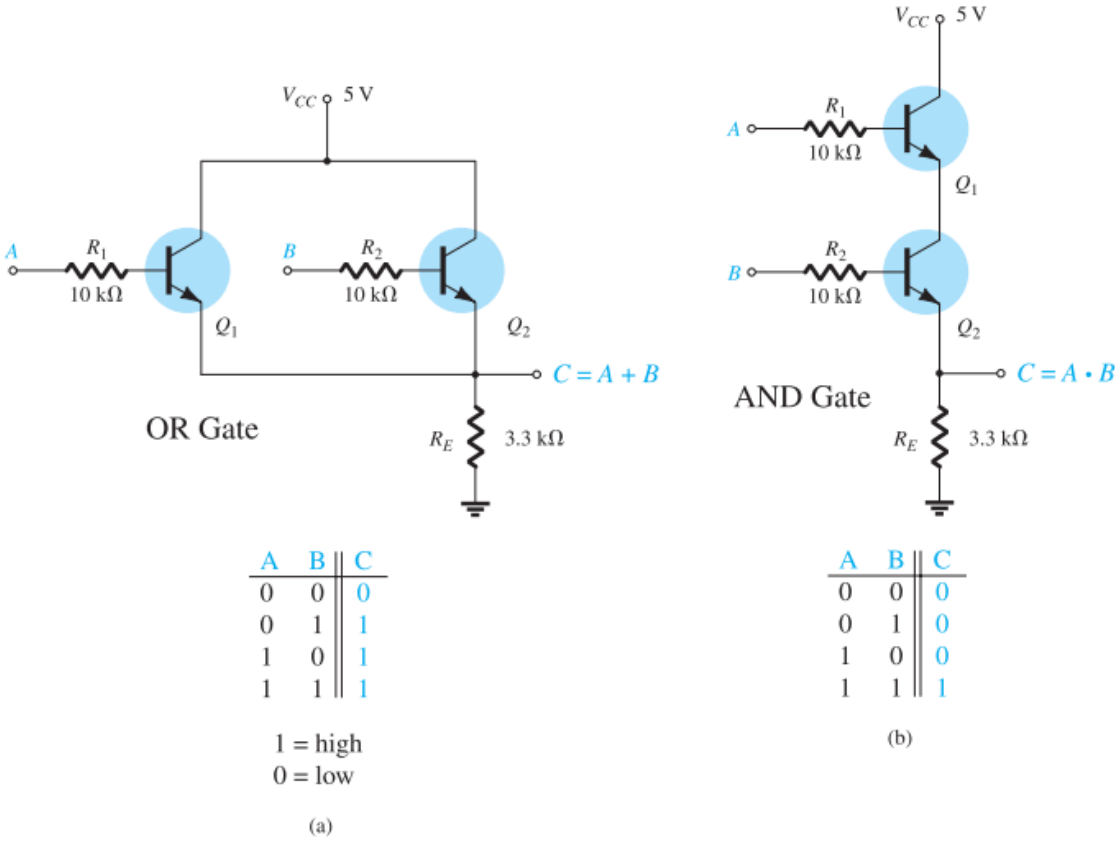


FIG. 4.111
BJT logic gates: (a) OR; (b) AND.

- For more details, refer to:
  - Chapter 3 & 4, Electronic Devices and Circuits, Boylestad.
- The lecture is available online at:
  - https://speakerdeck.com/ahmad_elbanna
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg